| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/715,778 | 11/17/2000 | Jack B. Dennis | 2222.4220001 | 7027 |

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| EXAMINER |
|---|
| MEW, KEVIN D |

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| 2616 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 09/715,778 | DENNIS, JACK B. |
| | Examiner | Art Unit | |
| | Kevin Mew | 2616 | |

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on <u>28 September 2007</u>.

2a)☐ This action is **FINAL**.          2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
    closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) <u>1-30</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-30</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
          application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

## Detailed Action

## Response to Amendment

1.     Applicant's Arguments/Remarks filed on 9/28/2007 regarding claims 1-30 have been

considered.  Claims 1-30 are currently pending.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.     **Claims 1-5, 8-9, 11-15, 18-19, 21-25, 28-29** are rejected under 35 U.S.C. 102(e) as being

anticipated by Whittaker et al. (USP 5,968,167).

Regarding claims 1, 11, 21, Whittaker discloses an apparatus to perform a method (an

apparatus, Fig. 1) comprising:

a processor (a combination of media control core 2, data processing units 6 and multi-

bank cache 14, col. 3, lines 20-21 and 29-31, elements 2, 6 and 14, Figs. 1 and 6) capable of

simultaneous execution of two or more threads of instructions (simultaneous execution of

threads, Fig. 6), wherein the processor (the combination of media control core 2, data processing

units 6 and multi-bank cache 14, col. 3, lines 20-21 and 29-31, Figs. 1 and 6) comprises:

at least two resource units (comprises a plurality of data processing units 6 and multi-

bank cache 14, col. 7, lines 61-67, col. 8, lines 1-8, and Fig. 1) capable of being assigned to an

instruction of each of the threads (capable of being assigned to each instruction of each thread,

col. 7, lines 61-67, col. 8, lines 1-8 and Fig. 6), wherein each of the resource units (each of the

data processing units 6 and bank cache 14, Fig. 1) is configured to implement only a subset of

instruction types of an instruction set (is configured to implement only a subset of instruction

types, such as video input processing, of an instruction set, col. 4, lines 4-54, col. 10, lines 15-24;

for example, an appropriate data processing unit and a particular cache bank will be instructed

and identified by the media control core to perform only video input/real-time data processing,

which is a subset of instruction types; the instruction set can comprise video as well as audio);

a priority register (resource checker, element 81, Fig. 6) to store thread information for

the threads (stores thread information such as pipeline data bank status and status of various data

processing units, col. 8, lines 18-28 and Fig. 6), the thread information including a priority code

corresponding to the instructions of each thread (the thread information including priority of

each thread corresponding to the instructions of each thread, see col. 8, lines 28-40), at least one

of the threads requesting use of one of the resource units (a thread requests use of a data

processing unit and a bank cache, Fig. 6) for processing a current instruction (for processing an

instruction, col. 4, lines 4-54, col. 10, lines 15-24); and

a priority selector (priority selector, col. 8, lines 28-32 and element 82, Fig. 6) coupled to

the priority register (coupled to the resource checker, Fig. 6) to generate assignment signal to

assign the resource units to the requesting thread's current instruction (assigns the appropriate

data processing unit to the requesting thread's instruction, col. 7, lines 61-67, col. 8, lines 1-8 and

Fig. 1) according to the P priority codes (according to the priority of each thread, col. 8, lines 18-

35).

Regarding claims 2, 12, 22, Whittaker discloses the apparatus of claim 1 to perform the method of claim 11 wherein each of the resource units is one of an instruction unit, a memory locking unit, a load unit, a store unit (multi-bank cache 14, col. 7, lines 61-67, col. 8, lines 1-8, and Fig. 1), an input/output unit, a peripheral unit interface, and a functional unit (data processing unit 6, col. 7, lines 61-67, col. 8, lines 1-8, and Fig. 1).

Regarding claims 3, 13, 23, Whittaker discloses the apparatus of claim 2 to perform the method of claim 12 wherein the functional unit is one of an arithmetic unit, a logic unit, and an arithmetic and logic unit (data processing unit functions an ALU, col. 12, lines 21-25).

Regarding claims 4, 14, 24, Whittaker discloses the apparatus of perform the method of claims 1 and 11, further comprising:

an instruction multiplexer (a plurality of instruction buffers, Fig. 6) coupled to the priority selector (priority selector, element 82, Fig. 6) to pass instructions stored in a plurality of instruction registers (to pass instructions stored in the instruction buffers to a plurality of resource checkers, col. 8, lines 18-35 and Fig. 6) to execution units according to the assignment signal (to the data processing units for execution according to the priority, col. 8, lines 30-32 and Fig. 1).

Regarding claims 5, 15, 25, Whittaker discloses the apparatus to perform the method of claims 1 and 11 further comprising:

a priority assignor (priority selector, see col. 8, lines 18-28) coupled to the priority

register (the resource checker) to set the thread information including at least one of the P

priority codes corresponding to the instructions of each thread (sets a priority to each thread

according to the thread instruction, col. 8, lines 18-31) in response to a start instruction from an

instruction decoder and dispatcher (in response to whether an instruction can run or not from an

combinatorial logic, col. 8, lines 2-8, 24-28).


Regarding claims 8, 18, 28, Whittaker discloses the apparatus to perform the method of

claims 1, 11, 21 above, wherein the priority selector is configured to assign one of the resource

units to the instructions of one of the threads (assigns an appropriate data processing unit to

instructions of each thread, col. 7, lines 61-67, col. 8, lines 1-8, and Fig. 1) if the one of the

threads is not served (if video input is not served, col. 4, lines 15-25) and the one of the resource

units is free (determines if the data bank is available, col. 3, lines 66-67, col. 4, lines 1-7).


Regarding claims 9, 19, 29, Whittaker discloses the apparatus to perform the method of

claims 8, 18, 28 above, wherein the one of the threads has highest priority code among a set of

ready threads (one of the threads has the highest priority, col. 8, lines 28-35).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains.  Patentability shall not be negatived by the
> manner in which the invention was made.

3.        Claims 6-7, 10, 16-17, 20, 26-27, 30 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Whittaker in view of Cutler et al. (USP 5,752,031).

Regarding claims 6, 16, 26, Whittaker discloses all the aspects of the claimed invention

set forth in the rejection of claims 5, 15, 25 above, except fails to explicitly show the apparatus to

perform the method wherein the priority assignor is configured to set an active flag in the priority

register corresponding to the at least one of the threads in response to the start instruction.

However, Cutler discloses a method and system for scheduling the execution of a

plurality of threads in a computer system such that it will set the flag to running/active state

when it receives a start execution instruction (element 40d, Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the multithreaded data processing management system of

Whittaker with the teaching of Cutler in set a thread to an running/active state in response to an

execution instruction such that Whittaker resets the active flag in the instruction buffer

corresponding to the at least one of the threads in response to a quit instruction from the

instruction decoder and dispatcher.  The motivation to do so is to keep track of the number of

currently active threads and ensure the number of active threads is at or near a predetermined

target level of concurrency.

Regarding claims 7, 17, 27, Whittaker discloses all the aspects of the claimed invention set forth in the rejection of claims 6, 16, 26 above, except fails to explicitly show the apparatus to perform the method wherein the priority assignor is configured to reset the active flag in the priority register corresponding to the at least one of the threads in response to a quit instruction from the instruction decoder and dispatcher.

However, Cutler discloses resetting the state of a thread to a terminated state when it receives an execution completion instruction (element 40g, Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the multithreaded data processing management system of Whittaker with the teaching of Cutler in resetting the flag for a thread to a terminated state when it receives an execution completion instruction such that Whittaker resets the active flag in the instruction buffer corresponding to the at least one of the threads in response to a quit instruction from the instruction decoder and dispatcher. The motivation to do so is to keep track of the number of threads that are still currently active and ensure the number of active threads is at or near a predetermined target level of concurrency.

Regarding claims 10, 20, 30, Whittaker discloses all the aspects of the claimed invention set forth in the rejection of claims 8, 1, 28 above, except fails to explicitly show the apparatus to perform the method wherein the priority selector is configured to iteratively assign resource units to instructions of threads in the set of ready threads according to the corresponding priority codes and resource availability until the set becomes empty.

However, Cutler discloses that the kernel schedules a processing unit and works its way

down from a higher priority thread of ready state to a lower priority thread of ready state (col. 10,

lines 43-45, col. 11, lines 4-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the multithreaded data processing management system of

Whittaker with the teaching of the system of Cutler in scheduling a processing unit and working

its way down from a higher priority thread of ready state to a lower priority thread of ready state

such that the priority selector of Whittaker will iteratively assign resource units to threads in the

set of ready threads according to the corresponding priority codes and resource availability until

the set becomes empty.

The motivation to do so is to use a priority scheme to determine the order in which

threads should execute, scheduling higher priority threads for execution before those with lower

priorities.


### *Response to Arguments*

4.      Applicant's arguments filed on 9/28/2007 have been fully considered but are moot in

view of the new ground(s) of rejection.

*Conclusion*

5.      Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kevin Mew whose telephone number is 571-272-3141.  The

examiner can normally be reached on 9:00 am - 5:30 pm.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chi Pham can be reached on 571-272-3179.  The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

        Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system.  Status information for published applications

may be obtained from either Private PAIR or Public PAIR.  Status information for unpublished

applications is available through Private PAIR only.  For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

                                                /Chi H Pham/
                                                Supervisory Patent Examiner, Art Unit
                                                2616
                                                5/20/08

        Kevin Mew    /K. M./
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